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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,042	03/12/2004	David A. Knol	X-1862-1P US	8589

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,042	KNOL ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/03/04,12/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/800,042 filed on 03/12/2004. Claims 1-7 remain pending in the application.

Specification

2. The disclosure is objected to because of the following informalities: the cross-reference information must be updated.

Appropriate correction is required.

Claim Objections

3. Claim 1 is objected to because following informalities:

line 2 replace "(thereafter pblock)" with –(pblock)--;

line 10 replace "a pcellview" with – a physical block cellview (a pcellview) --.

4. Claim 4 is objected to because following informalities:

line 2 replace "(thereafter pcellview)" with –(pcellview) --;

line 7 replace "(said netlist)" with – a netlist--;

line 12, Applicant must clarify "internal pins" (of what?- of said pblock?).

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being unpatentable by Williams (US Patent 6,631,508).

6. As to claims 1, 4-7 Williams discloses:

(1) A computer readable medium having stored thereon a data structure defining a physical block (hereafter pblock) in a hierarchy of pblocks which defines the same integrated circuit structure by reference to data in a netlist which defines a logical hierarchy, the data defining said pblock comprising (col.7, ll.5-14; col.7, ll.27-32):

A) a field or list containing pointers to data defining boundary pins or said pblock (A floorplan_element data structure includes a physical_container and pointers to adjacent (north, south, east, west) floorplan_elements – col.12, ll.57-59) or containing data which defines boundary pins assigned to said pblock, said boundary pins for connecting to external nets (col.12, ll.21-43; col.12, ll.55-64);

B) a field containing a pointer to a parent cellview which contains said pblock (The parameter, parent, identifies the container that is to receive the container identified by the parameter, child – col.11, ll.16-17; The primitives of a design can be uniquely identified by the unique positions of the primitives in the design's logical hierarchy. For example, the message "g0(1):g01:u1 [muxcy]" indicates that there is a primitive in this design of type muxcy which can be found in the logical hierarchy at location "g0(1):g01:u1". This primitive also exists in the physical hierarchy at location "testbench: uut3" –col.20, ll.54-60, Fig. 5) (col.11, ll.10-20; col.20, ll.54-60);

C) a field containing a pointer to a pcellview data structure owned by said pblock, said pcellview containing data or pointers to data which define lists of pins, nets, child pblocks and child instances which have been assigned to said pblock and which define the functionality of said pblock (Design objects are allocated to parent containers by identifying their unique position in the design's logical hierarchy. When a design object is assigned to a container in this fashion, a placement relationship must be provided to establish the object's position with respect to the other objects assigned to that container. A container is a 2-dimensional, square or rectangular boundary that has dimensions sufficient to enclose any containers designated as its "children". The dimensions of the child containers and the placement relationships that have been established between the children containers dictate the dimensions of the parent col.7, ll.57-67; col.8, ll.1-3) (col.2, ll. 61- 67; col.3, ll.1-16; col.5, ll.15-35; col.7, ll.55-67; col.8, ll.1-3; col.9, ll.55-62); and

D) a field containing coordinates on a floorplan representing a surface of an integrated circuit on which said circuits assigned to said pblocks are to be formed, said coordinates being such as to define a geometric shape representing said pblock and the size thereof (The database 258 that maintains the information about the physical location of the design's primitives consists of a map of an empty chip. The map's dimensions are adjusted while performing the calculate_container_dimensions procedure so that the map is always just big enough to hold the full extent of the layout. A floorplan element is essentially a place-holder for primitives. For example, in the case of a Virtex FPGA, the floorplan element is a CLB. For other devices, the floorplan

element is something different. Once a floorplan element is available at the desired coordinate, the place_primitives command is used to place the specified primitive in the floorplan element – col.11, ll.46-59), said geometric shape being displayed on a computer display of a computer executing a floor planning process (all the details of the square area bounded by the physical design's rectangular dimensions are shown in the CLB view of the display of FIG. 6-col.21, ll.12-14) (col.9, ll.29-45; col.11, ll.46-67; col.20, ll.61-67; col.21, ll.1-14);

(4) computer readable medium having stored thereon a data structure defining a physical block cellview (pcellview) owned by a particular pblock in a hierarchy of pblocks which defines the internals (objects) of said pblock which owns said pcellview, the data defining said pcellview comprising:

A) a list containing data which defines a list of pblocks which are included or nested within said pblock defined by data elements A through D (col.11, ll.10-20; col.12, ll.21-43; col.12, ll.55-64; col.20, ll.54-60);

B) a list containing data or pointers to data On said netlist which define instances which have been assigned to said pblock (col.3, ll.4-16; col.5, ll.15-34);

C) a list containing data or pointers to data which define boundary pins of said pblock which connect to internal nets of said pcellview (col.5, ll.15-34; col.13, ll.11-30);

D) a list containing data or pointers to data which define internal physical nets which connect from boundary pins of said pblock to internal pins so as to complete the original connectivity between instances defined in said netlist (col.5, ll.15-34; col.13, ll.11-30); and

E) a field which contains a pointer to a data object representing a parent pblock that envelopes the pcellview data object defined by data elements A through E (col.11, ll.10-20; col.20, ll.54-60);

(5) A computer readable medium having stored thereon a data structure defining an array that links instances from a netlist to pblocks of a physical hierarchy, said array comprising: a plurality of rows of a one column table, each row having an index that corresponds to a particular instance from a logical netlist, with the entry in the single column at that row comprising a field which contains a pointer to a pblock in a physical hierarchy of pblocks to which is assigned the instance corresponding to said row (The primitives of a design can be uniquely identified by the unique positions of the primitives in the design's logical hierarchy. For example, the message "g0(1):g01:u1 [muxcy]" indicates that there is a primitive in this design of type muxcy which can be found in the logical hierarchy at location "g0(1):g01:u1". This primitive also exists in the physical hierarchy at location "testbench: uut3") (col.20, ll.54-60);

(6) A computer readable medium having stored thereon a data structure defining a floorplan for circuits integrated on an integrated circuit and assigned to physical blocks (pblocks) in a physical hierarchy of pblocks, comprising:

an array containing: a plurality of rows of a one column table, each row having an index that corresponds to a particular instance from a logical netlist, with the entry in the single column at that row comprising a field which contains a pointer to a pblock in a physical hierarchy of pblocks to which is assigned the instance corresponding to said row (col.20, ll.54-60);

a field containing an identifier of a root pblock which is a pblock which will contain all other pblocks in a physical hierarchy of pblocks (col.11, ll.10-20; col.20, ll.36-60);

(7) A computer readable medium having stored thereon a data structure defining a physical net coupled to instances in physical blocks (pblocks) in a physical hierarchy of pblocks, comprising:

a field containing a pointer to a parent Pcellview to which a physical net defined by said data structure belongs (col.5, ll.15-34;col.11, ll.10-20; col.13, ll.11-30; col.20, ll.54-60);

a list containing pointers to data objects defining physical boundary pins to which said physical net is coupled in said physical hierarchy or data directly defining said boundary pins (col.5, ll.15-34; col.13, ll.11-30); and

a list containing pointers to data objects of a logical netlist which define logical netlist pins on instances in said logical netlist to which said physical net is coupled in said physical hierarchy or data directly defining said logical netlist pins (col.5, ll.15-34; col.13, ll.11-30; col.20, ll.54-60).

7. As to claims 2-3 Williams recites:

(2) The computer readable medium, wherein said field or list also contains pointers to data, which define internal pins of instances (objects), contained within said pblock (col.2, ll. 61- 67; col.3, ll.1-16; col.5, ll.15-35; col.7, ll.55-67; col.8, ll.1-3; col.9, ll.55-62);

(3) The computer readable medium, wherein said data structure includes a pcellview data structure comprising a field which contains a pointer to a data object

representing a parent defined by data elements of claim 1 (col.2, ll. 61- 67; col.3, ll.1-16; col.5, ll.15-35; col.7, ll.55-67; col.8, ll.1-3; col.9, ll.55-62; col.11, ll.10-20; col.12, ll.21-43; col.12, ll.55-64; col.20, ll.54-60).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NL

Thuan Do
THUAN DO
Primary examiner.
3/30/06